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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,081	11/19/2003	Motohiko Bungo	P03-1003	7003

56026 7590 11/28/2005

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EXAMINER

SCHLIE, PAUL W

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/717,081	Applicant(s) BUNGO, MOTOHIKO	
	Examiner Paul W. Schlie	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-11 have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Fukazawa (JP09212615).

As per claim 1, Fukazawa teaches a memory module indicator device having an indicator circuit using an indicator element to indicate the type and frequency of access to semiconductor memory composing a standardized memory module (see figures 4-5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukazawa (JP09212615) in further in view of Perron III (4,919,030).

As per claim 2 and 4-9, being dependant on claim 1, 8, or corresponding dependants inclusively; Fukazawa does not teach that an indicator device may count, display, and "hold" an indication corresponding to the maximum frequency of access

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corresponding to an access type measured within a period of time utilizing multiple display elements; wherein a divided clock signal may serve as the basis of a periodic time reference, and a common counter circuit may be multiplexed in such a manner that it may determine the count/frequency of each access type measured in alternating periods of time. However Perron III teaches an visual indicator device composed of a common counter circuit which may measure a frequency by way of counting events within a periodic interval, and a display and "hold" a representation of the maximum count representing that frequency utilizing common counters, and indicators (see figure 1 Counter A, Latch A and element 388), and which may be further adapted by what is considered to be common knowledge to one of ordinary skill in the art (and for which official notice of this view is given) to multiplex a common counter circuit element between multiple latched indicators utilizing a periodic signal derived from a divided down reference clock signal such that a representation of an arbitrary number of signal frequencies measured and correspondingly alternately indicated. It would be obvious to one of ordinary skill in the art to combine that which these references teach, for the benefit of being able to display multiple individual access type frequencies in a cost and power efficient manner.

6. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukazawa (JP09212615) and Perron III (4,919,030) in further view of McNamara (3,904,861).

As per claims 3 and 10, being dependant on claims 1 or 9 respectively, neither Fukazawa or Perron III teach a circuit board with correspondingly compatible

connectors which may be placed between a memory module and motherboard thereby interconnecting the memory module to the mother board, and enabling a memory module indicator device to access the signals required to indicate the type and frequency of memory module access as may be desired. However, McNamara teaches such and adaptor/extender circuit board which may further host other circuit elements and/or indicators (see figures 2-3 elements 25 and 30-36, and column 3 lines 56-62).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukazawa (JP09212615), Perron III (4,919,030) and McNamara (3,904,861) in further view of themselves.

As per claim 11, being dependent on claim 10, although Fukazawa, Perron III, nor McNamara teaches a adaptor/extender board assembly comprising mating memory module and corresponding motherboard connectors, and be itself integral to a memory access indicator device to enable the display of a standardized memory module's access type frequencies; official notice is given that it is considered obvious to one of ordinary skill in the art to enable an indicator element sub-assembly to be mounted remotely by interconnecting it to it's origin of control utilizing a common signal cable and corresponding connectors. It would be obvious to one of ordinary skill in the art at the time of invention to modify the combined cited reference elements by interconnecting indicator elements to the cited adaptor/extender board comprising the display device through a signal cable and corresponding connector, for the benefit of being able to mount the display element remotely.

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


PIERRE BATAILLE
PRIMARY EXAMINER